Functional Materials

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Estimation of medium-range strain in 3D-stacked silicon-based integrated circuits using energy filtered CBED

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A current trend in semiconductor industry is 3D-stacking of integrated circuits using Through Silicon Vias (TSVs) in order to reduce floor space, to reduce power loss and to increase bandwidth. Due to the different coefficients of thermal expansion (CTE) of the involved materials, especially silicon as substrate and copper as the conducting via, transistors that are located next to a TSV in a range of some micrometers are affected by the resulting stress [1]. That means, this additional stress component and the stress in the transistor channel of MOSFETs – as performance booster in leading-edge devices [2] – and can influence the device performance. Strain measurements in channel regions of some 10 nm are necessary to understand the effect of strain on transistor performance – as one factor in addition to other sources like patterning effects, dopand fluctuations etc. – and to validate models used for performance simulation of 3D-stacked ICs [2].

Besides the direct imaging of strained lattice planes in HRTEM, the geometrical phase analysis (GPA) using inline holography [3] or off-axis holography [4] and diffraction-based methods are able to determine strain in crystalline materials. Whereas GPA requires a region with a well known strain situation in the vicinity of the ROI, for diffraction-based methods this reference region should be available for the TEM study without exchanging the specimen. Nano Beam Diffraction (NBD) is suitable for the determination of short-range strains in the silicon transistor channel [5, 6]. Conversion Beam Electron Diffraction (CBED) analysis uses a larger, medium-range region, i. e. strain measurements are performed on micrometer scale, but provides lattice parameter with high accuracy [7].

Usually the CBED measurement requires simulations of the High Order Laue Zone (HOLZ) pattern for exact adjustment of the actual acceleration voltage and of the strain state [8]. For well-defined stress states like a uniaxial strain state, the strain is usually calculated directly from the measured values. The reciprocal value of the Kikuchi line distance is proportional to the lattice plane. The use of an in-column energy filter improves the signal-to-noise ratio of the diffraction pattern, and the application of a sub-pixel peak fitting procedure leads to a precision better than 4×10^{-4}, covering the expected order of magnitude of strain (Fig. 1).

Measurements of lattice strain along a vertical line demonstrate that the level of strain beneath a transistor remains constant at a level of 0.3µm below the Si-upper edge. Based on the layout of the chip, locations 500nm below the bottom of the Shallow Trench Isolation (STI) were chosen for the strain measurement, for 3 transistors with different distances to the TVS. In addition, the strain course across the lamellae was measured (Fig. 2). The reference value was measured using an extraordinary lamella at a location where no strain due to influences of functional structures in the chip is expected.

The results were compared with simulations based on materials parameters and geometrical data of the whole TEM specimen. The measured strain values provide a basis for model validation and calibration.

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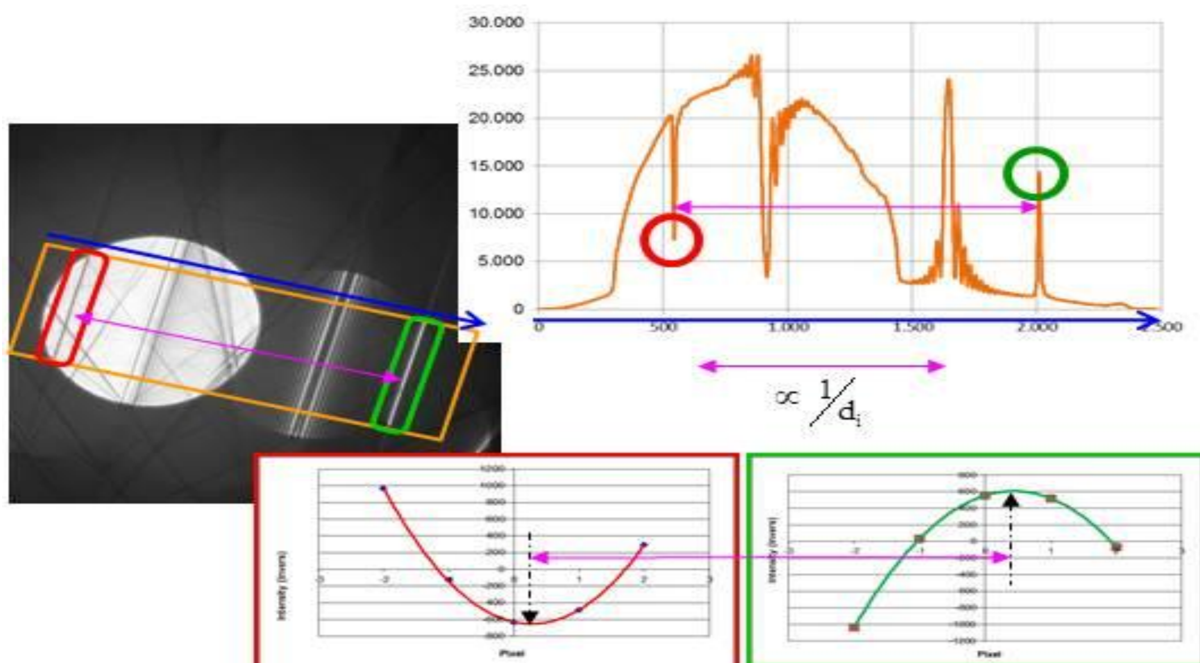

Figure 1. Methodology of strain measurement base on Kikuchi line spacing: left: CBED pattern Up: Intensity profile, bottom: fit with sub-pixel precision of dark and bright Kikuchi line, leading to reciprocal d values

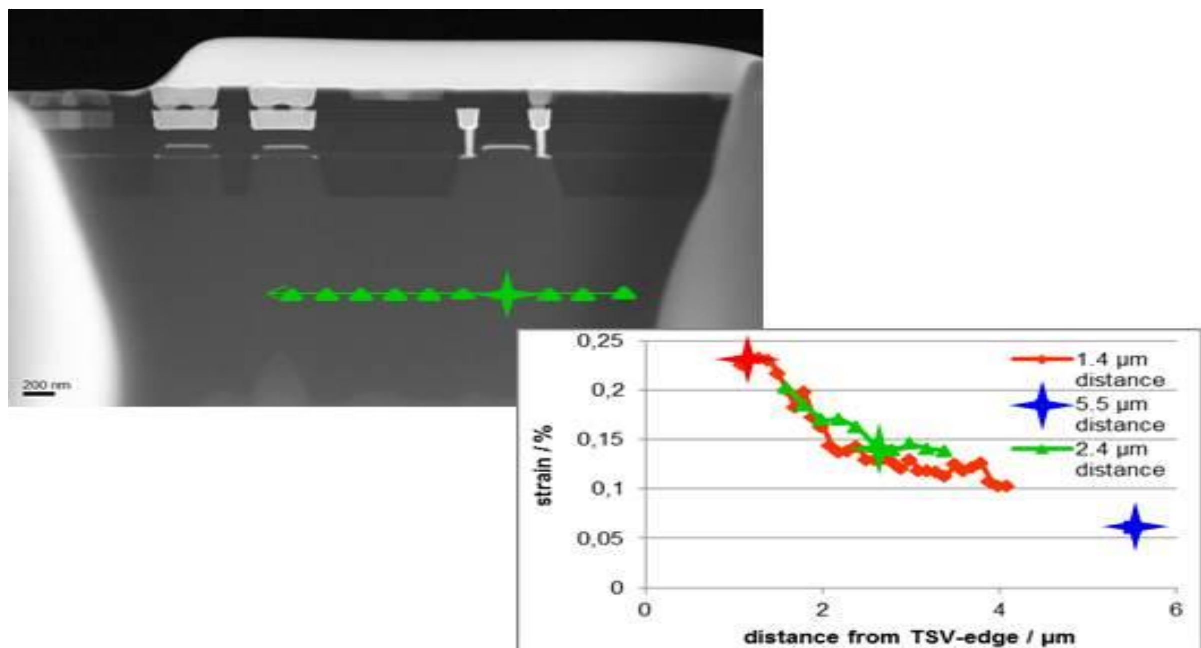

Figure 2. HAADF-STEM imaging of a transistor (left) with marked locations of measurement, and the trace across the TEM-lam.